Listing of Claims to Show Changes Made to the Claims

1.(original) A phase division multiple access (PDMA) system, the system comprising:

at least one receiver logic combiner, the at least one receiver logic combiner adapted to generate a plurality of composite PN codes, wherein each of the plurality of composite PN codes are separated by a predetermined PN phase.

2.(original) A PDMA system as in claim 1, further comprising at least three first receiver pseudo-noise (PN) component code generators coupled to the at least one receiver logic combiner, wherein each of the at least three first receiver pseudo-noise (PN) component code generators generate relatively prime PN component codes.

3.(original) A PDMA system as in claim 2 further comprising at least one PN phase delayer coupled to one of the at least three first receiver PN component code generators.

4.(original) A PDMA system as in claim 2 wherein the at least three first receiver pseudo-noise (PN) component code generators comprise four first receiver PN component code generators.

5.(original) A PDMA system as in claim 1 wherein the predetermined PN phase substantially equals at least one PN minor epoch.

6.(original) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MAND logic combiner.

7.(original) A PDMA system as in claim 1 wherein the eceiver logic combiner comprises a MAJ logic combiner.

8.(original) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MOD logic combiner.

9.(original) A method for generating multi-phase composite pseudo-noise (PN) codes, the method comprising:

generating a first composite PN code; and

generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code.

10.(original) A method as in claim 9 wherein generating the first composite PN code comprises:

generating a plurality of relatively prime PN component codes;

PN phase delaying one of the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

11.(original) A method as in claim 10 wherein generating the second composite PN code comprises:

generating the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

12.(original) A method as in claim 9 wherein generating the second composite PN code further comprises generating the second composite PN code at least one PN minor epoch phase separated from the first composite PN code.

13.(original) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MOD combining the plurality of relatively prime PN component codes.

14.(original) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MAJ combining the plurality of relatively prime PN component codes.

15.(original) A method as in claim 10 wherein combining the plurality of relatively prime PN component codes further comprises MAND combining the plurality of relatively prime PN component codes.

16.(original) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes further comprises MOD combining the plurality of relatively prime PN component codes.

17.(original) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes further comprises MAJ combining the plurality of relatively prime PN component codes.

18.(original) A method as in claim 11 wherein combining the plurality of relatively prime PN component codes further comprises MAND combining the plurality of relatively prime PN component codes.

19.(original) An integrated circuit (IC), wherein the IC comprises:

at least three receiver pseudo-noise (PN) component code generators PN_x, PN_y, PN_z, wherein each PN component code generator is adapted to generate relatively prime PN component codes when compared with each of the other PN component code generators;

a PN phase delayer Z_d coupled to one of the at least three receiver PN component generators; and

at least one receiver logic combiner coupled to the at least three receiver pseudo-noise (PN) component code generators PN_x, PN_y, PN_z, and the PN phase delayer Z_d, wherein the at least one receiver logic combiner is adapted to generate a plurality of composite PN codes separated by a PN phase determined by PN phase delayer Z_d.

20.(currently amended) An IC as in claim [[13]] 19 wherein the IC comprises an Application Specific IC (ASIC).

21.(currently amended) An IC as in claim [[13]] 19 wherein the IC comprises a field programmable gate array (FPGA).

22.(original) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes, the method comprising:

generating a first composite PN code, wherein generating the first composite PN code comprises:

generating a plurality of relatively prime PN component codes;

combining the plurality of relatively prime PN component codes;

generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code wherein generating the second composite PN code comprises:

generating the plurality of relatively prime PN component codes;

PN phase delaying one of the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

23.(original) A program storage device as in claim 22 wherein the program of instructions comprises at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

Respectfully submitted,

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